WHAT IS CLAIMED IS:

1. A flip chip semiconductor device of a multi-layered structure having a cell forming layer and a pad forming layer, comprising:

input and output cells formed in said cell forming layer together with macro-cells;

power supply pads formed in said pad forming layer, and electrically connected to said input and output cells; and

signal pads formed in said pad forming layer, electrically connected to said input and output cells, and arranged outside of said power supply pads.

2. The flip chip semiconductor device as set forth in claim 1, in which said signal pads and said power supply pads are to be connected to corresponding signal pads directly connected to signal lines without passing through a different layer and corresponding power supply pads formed on a pad forming layer of a multi-layered package substrate.

3. The flip chip semiconductor device as set forth in claim 1, in which said input and output cells form input and output cell groups which in turn form columns of input and output cell groups extending in directions crossing peripheral edges of said pad forming layer.

4. The flip chip semiconductor device as set forth in claim 3, in which said directions are perpendicular to said peripheral edges of said pad forming layer shaped in a rectangular configuration.

5. The flip chip semiconductor device as set forth in claim 3, in which said signal pads and said power supply pads are to be connected to corresponding

signal pads directly connected to signal lines without passing through a different layer and corresponding power supply pads formed on a pad forming layer of a multi-layered package substrate.

6. The flip chip semiconductor device as set forth in claim 3, in which said signal pads form column groups of signal pads respectively associated with said columns of input and output cell groups.

7. The flip chip semiconductor device as set forth in claim 6, in which each of said column groups of signal pads has a column of signal pads located over associated one of said columns of input and output cell groups and other columns of signal pads adjacent to said column of signal pads.

8. The flip chip semiconductor device as set forth in claim 7, in which said other columns of signal pads are symmetrically arranged on both sides of said column of signal pads.

9. The flip chip semiconductor device as set forth in claim 7, in which said other columns of signal pads are asymmetrically arranged with respect to said column of signal pads.

10. The flip chip semiconductor device as set forth in claim 6, in which one of said column groups of signal pads includes a column of signal pads located over associated one of said columns of input and output cell groups and at least one column of signal pads located on either side of said column of signal pads.

11. The flip chip semiconductor device as set forth in claim 1, in which said macro-cells are formed inside of said input and output cells.

12. The flip chip semiconductor device as set forth in claim 3, in which said columns of input and output cell groups are spaced from one another so that said macro-cells arranged in such a manner as to occupy an inner area of said cell forming layer and vacant areas between said columns of input and output cell groups.

13. The flip chip semiconductor device as set forth in claim 3, in which said input and output cell groups are equal in the number of said input and output cells to one another.

14. The flip chip semiconductor device as set forth in claim 3, in which at least one of said input and output cell groups is different in the number of said input and output cells from others of said input and output cell groups.

15. The flip chip semiconductor device as set forth in claim 3, in which said columns of input and output cell groups are equal in the number of said input and output cell groups to one another.

16. The flip chip semiconductor device as set forth in claim 3, in which at least one of said columns of input and output cell groups is different in the number of said input and output cell groups from others of said columns of input and output cell groups.

17. The flip chip semiconductor device as set forth in claim 3, in which at least two of the input and output cells of one of said input and output cell groups are spaced from one another.

18. The flip chip semiconductor device as set forth in claim 3, in which at least one of said input and output cell groups is constituted by only one input and output cell.

19. The flip chip semiconductor device as set forth in claim 3, in which at least one of said input and output cell groups has one of the input and output cells and other input and output cells symmetrically arranged with respect to said one of said input and output cells.

20. The flip chip semiconductor device as set forth in claim 3, in which at least one of said input and output cell groups has one of the input and output cells and other input and output cells asymmetrically arranged with respect to said one of said input and output cells.

21. The flip chip semiconductor device as set forth in claim 3, in which one of said columns of input and output cell groups has the input and output cell groups contiguous to one another.

22. The flip chip semiconductor device as set forth in claim 3, in which one of said columns of input and output cell groups has the input and output cell groups spaced from one another for providing a vacant area assigned to a wiring line.

23. The flip chip semiconductor device as set forth in claim 3, in which the input and output cell groups are removed from at least one of said columns of input and output cell groups so that the macro-cells occupy the vacancy of an area to be assigned to said at least one of said columns of input and output cell groups.

24. The flip chip semiconductor device as set forth in claim 3, in which said columns of input and output cell groups are arranged at regular intervals.

25. The flip chip semiconductor device as set forth in claim 3, in which two of said columns of input and output cell groups are spaced by an interval different from the interval between other two of said columns of input and output cell groups.

26. The flip chip semiconductor device as set forth in claim 3, in which said columns of input and output cell groups are powered through power supply lines connected to said power supply pads through via-holes and extending in parallel thereto.

27. The flip chip semiconductor device as set forth in claim 1, in which the power supply pads connected to said input and output cells are arranged on a virtual closed line extending inside of said signal pads.

28. The flip chip semiconductor device as set forth in claim 27, in which said virtual line outwardly projects at corners of said pad forming layer so as to extend outside of an area of said cell forming layer where said macro-cells occupy.

29. The flip chip semiconductor device as set forth in claim 1, further comprising power supply lines extending on a layer of said multi-layered structure different from said cell forming layer and said pad forming layer and connected at first ends thereof to said input and output cells at second ends thereof to said power supply pads together with power supply lines connected between other power supply pads and said macro-cells.

30. The flip chip semiconductor device as set forth in claim 3, in which one of said input and output cells in one of said input and output cell groups is different in size from other input and output cells in the same input and output cell group.